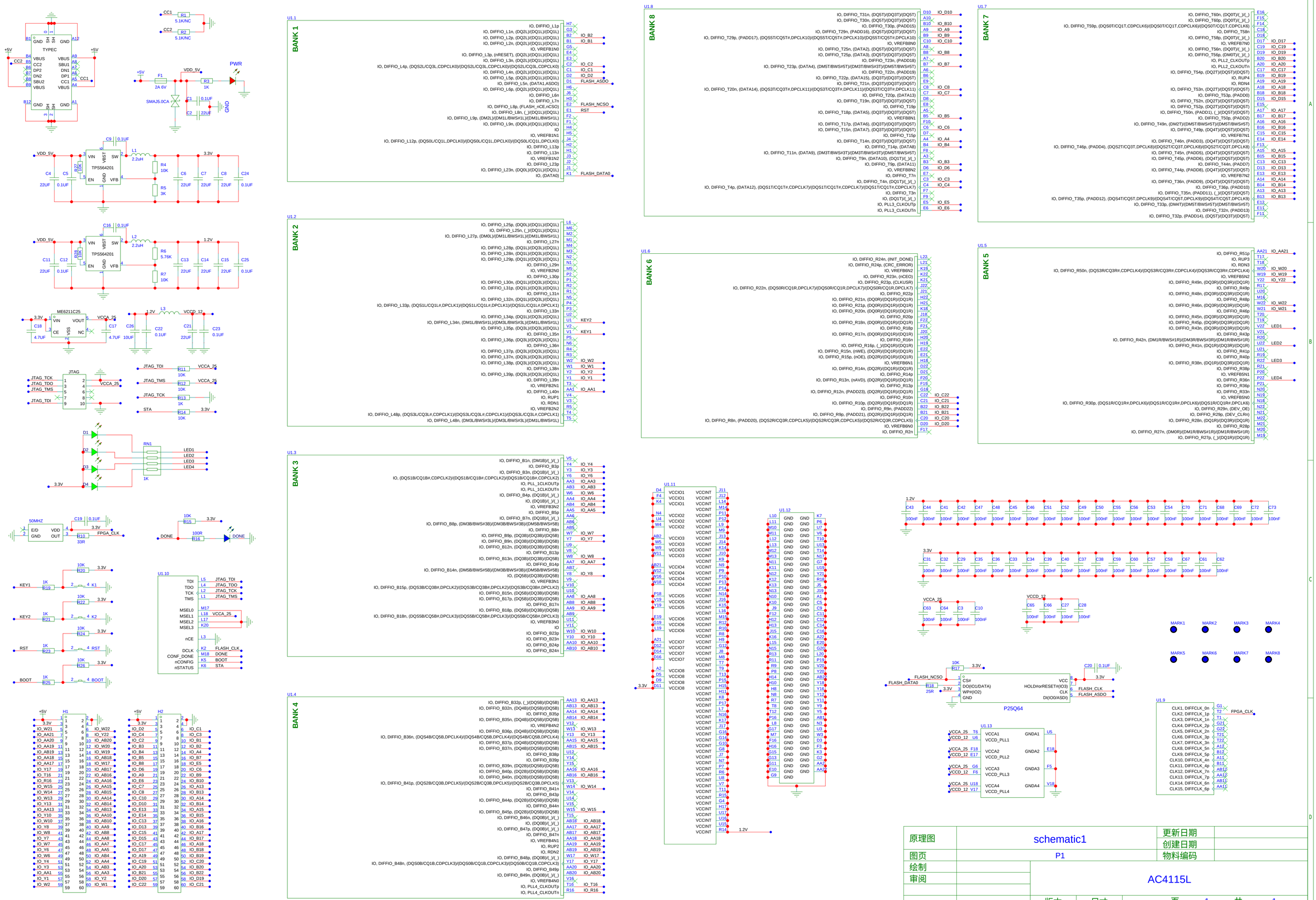
TYPEC
GND SH SH GND
VBUS CC2 DP2 DN2 SBU2 VBUS
VBUS SBU1 DN1 DP1 CC1 VBUS
CC1 CC2 VDD_5V
R1 5.1K/NC
R2 5.1K/NC
+5V
F1 2A 6V
SMAJ5.0CA
R3 1K
PWR
C1 0.1UF
C2 22UF
GND
VDD_5V
C9 0.1UF
VIN SW VBST EN GND VFB
TPS564201
L1 2.2uH
R27 10K
R4 10K
R5 3K
C4 22UF
C5 0.1UF
C6 22UF
C7 22UF
C8 22UF
C24 0.1UF
3.3V
C16 0.1UF
L2 2.2uH
R28 10K
R6 5.76K
R7 10K
C11 22UF
C12 0.1UF
C13 22UF
C14 22UF
C15 22UF
C25 0.1UF
1.2V
ME6211C25
VIN VOUT CE NC VSS
C18 4.7UF
C17 4.7UF
VCCA_25
L3
VCCD_12
C26 10UF
C22 0.1UF
C21 22UF
C23 0.1UF
JTAG
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
R11 10K
R12 10K
R13 1K
R14 10K
JTAG_TRS
STA
D1
D2
D3
D4
RN1
LED1
LED2
LED3
LED4
1K
50MHZ
E/D VDD GND OUT
C19 0.1UF
R10 33R
FPGA_CLK
R15 10K
R16 100R
DONE
KEY1
KEY2
RST
BOOT
R19 1K
R20 10K
R21 1K
R22 10K
R23 1K
R24 10K
R25 1K
R26 10K
K1
K2
TDI TDO TCK TMS
MSEL0 MSEL1 MSEL2 MSEL3
nCE
DCLK CONF_DONE nCONFIG nSTATUS
VCCA_25
FLASH_CLK
BOOT
H1
H2
U1.1
BANK 1
U1.2
BANK 2
U1.3
BANK 3
U1.4
BANK 4
U1.8
BANK 8
U1.7
BANK 7
U1.6
BANK 6
U1.5
BANK 5
U1.11
U1.12
U1.13
GNDA1 GNDA2 GNDA3 GNDA4
VCCA1 VCCD_PLL1
VCCA2 VCCD_PLL2
VCCA3 VCCD_PLL3
VCCA4 VCCD_PLL4
U1.10
U1.9
CLK1, DIFFCLK_0n
CLK2, DIFFCLK_1p
CLK3, DIFFCLK_1n
CLK4, DIFFCLK_2p
CLK5, DIFFCLK_2n
CLK6, DIFFCLK_3p
CLK7, DIFFCLK_3n
CLK8, DIFFCLK_5n
CLK9, DIFFCLK_5p
CLK10, DIFFCLK_4n
CLK11, DIFFCLK_4p
CLK12, DIFFCLK_7n
CLK13, DIFFCLK_7p
CLK14, DIFFCLK_6n
CLK15, DIFFCLK_6p
MARK1 MARK2 MARK3 MARK4
MARK5 MARK6 MARK7 MARK8
R17 10K
R18 25R
FLASH_NCSO
FLASH_DATA0
C20 0.1UF
CS# DO(IO1/DATA) WP#(IO2) GND
VCC HOLD#orRESET#(IO3) CLK DI(IO0/ASDI)
P25Q64
FLASH_CLK
FLASH_ASDO
原理图 schematic1
图页 P1
绘制
审阅
更新日期
创建日期
物料编码
AC4115L
版本 V1.0
尺寸 A3
页 1 共 1
思妙电子
SiMiaoHub